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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/739,226	12/19/2003	Kris W. Johnson	08350.3501	8495

58982 7590 01/08/2007

CATERPILLAR/FINNEGAN, HENDERSON, L.L.P.
901 New York Avenue, NW
WASHINGTON, DC 20001-4413

EXAMINER	
PATEL, DHARTI HARIDAS	
ART UNIT	**PAPER NUMBER**
2836	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/739,226	JOHNSON ET AL.	
	Examiner	Art Unit	
	Dharti H. Patel	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-2, 10-11, 14-15, 21, and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Parker, Patent No. 6,762,920.

With respect to claim 1, Parker teaches a current monitoring and interrupting circuit [Fig. 1, Fig. 2, Col. 1, lines 15-17] an electrically conductive line [Fig. 1, 1, line coming from VF AC] carrying a current; a sensor [Fig. 1, 13, Col. 3, lines 10-13] outputs a voltage level indicative of a magnitude of the current [Processor 11 of Fig. 1 includes analog circuitry 19 and microprocessor 21 shown in Fig. 2; Sensor 13 in Fig. 1 outputs a voltage level indicative of a magnitude of the current]; a comparator [Fig. 2, 55, Col. 3, lines 52-53] that compares the voltage level to a reference potential [Fig. 2, SDLYTRIPTHRESH] and generates a circuit indicator signal [Fig. 2, output from comparator 55]; and a logic-based current interrupter [Fig. 2, 57, Col. 3, lines 52-56] that controls the current in line [Fig. 1, 1, line coming from VF AC] in response to the circuit indicator signal.

With respect to claim 2, Parker further includes a current switch [Fig. 1, 5, 7] disposed in the electrically conductive line [Fig. 1, 1, line coming from VF AC] and connected to the logic-based interrupter [Fig. 2, 57, The trip latch 57 is connected to the operating mechanism 7, which is connected to a switch 5 as shown in Fig. 1].

With respect to claim 10, Parker teaches that the logic-based current interrupter includes a Boolean logic device [Fig. 2, 57, trip latch 57 is a Boolean logic device].

With respect to claim 11, Parker teaches that the Boolean logic device includes a flip-flop [Fig. 2, 57, trip latch 57 is a flip-flop].

With respect to claim 14, Parker teaches a method of monitoring and interrupting current [Fig. 1, Fig. 2, Col. 1, lines 15-17] flowing in an electrically conductive line [Fig. 1, 1, line coming from VF AC], comprising sensing the current [Fig. 1, 13, Col. 3, lines 10-13] flowing in the electrically conductive line; generating a voltage level indicative of a magnitude of the current [Processor 11 of Fig. 1 includes analog circuitry 19 and microprocessor 21 shown in Fig. 2; Sensor 13 in Fig. 1 outputs a voltage level indicative of a magnitude of the current]; comparing the voltage level [Fig. 2, 55, Col. 3, lines 52-53] to a reference voltage [Fig. 2, SDLYTRIPTHRESH] and generating a circuit indicator signal [Fig. 2, output from comparator 55]; and using a logic-based device [Fig. 2, 57, Col. 3, lines 52-56] to cause an interrupting of the current flowing in the electrically conductive line [Fig. 1, 1, line coming from VF AC] if the circuit

indicator signal is indicative of a condition where the voltage level is higher than the reference voltage.

With respect to claim 15, Parker teaches that the logic based device [Fig. 2, 55, Col. 3, lines 52-56] includes a flip flop that controls a current switch [Fig. 2, trip latch (flip flop) 57 controls the operating mechanism 7, which controls switch 5 in Fig. 1].

With respect to claim 21, Parker teaches a circuit breaker [Fig. 1, 3, Fig. 2] for interrupting a flow of current [Col. 1, lines 15-17] in an electrically conductive line [Fig. 1, 1, line coming from VF AC], comprising a sensor [Fig. 1, 13, Col. 3, lines 10-13] that outputs a voltage level indicative of a magnitude of the current [Processor 11 of Fig. 1 includes analog circuitry 19 and microprocessor 21 shown in Fig. 2; Sensor 13 in Fig. 1 outputs a voltage level indicative of a magnitude of the current]; a comparator [Fig. 2, 55, Col. 3, lines 52-53] that compares the voltage level to a reference potential [Fig. 2, SDLYTRIPTHRESH] and generates a circuit indicator signal [Fig. 2, output from comparator 55]; a logic device [Fig. 2, 57, Col. 3, lines 52-56] that receives the circuit indicator signal and generates a current interrupt signal when the circuit indicator signal corresponds to a condition where the voltage level is greater than the reference potential [Col. 3, lines 52-56]; and a current switch [Fig. 1, 5, 7, Fig. 2, 7] that selectively prevents the flow of current in the electrically conductive line in response to the current interrupt signal [Col. 3, lines 8-10].

With respect to claim 23, Parker teaches that the logic device [Fig. 2, 57] includes a flip-flop.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 3-4, 12-13, 16-19, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parker, in view of Canova et al., Publication No. US 2003/0202304.

Parker teaches a current switch [Fig. 1, 5], but does not disclose that the current switch includes a MOSFET. Conova teaches an electronic circuit breaker connecting a power-supply network and a load.

With respect to claim 3, Canova teaches that the current switch [Fig. 1, 7] includes a MOSFET [Page 2, paragraph 0020, lines 17-19].

Both teachings are analogous circuit breakers connected between power supply and loads. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Canova, which teaches a MOSFET switch, with the circuit of Parker, for the benefit of interrupting electric power supply to a user circuit when the current exceeds a pre-set value.

With respect to claim 4, Canova further includes a fuse [Fig. 1, 5, Page 1, paragraph 0020, lines 4-5, lines 3-7].

With respect to claim 12, Canova further includes a reset circuit [Page 1, paragraph 0012, lines 8-10, the microprocessor 13 in Fig. 1 comprises a reset circuit, which sends a reset signal to the circuit breaker].

With respect to claim 13, Canova further includes an indicator [Fig. 1, 3] that signals whether the current is flowing in the electrically conductive line [Page 1, paragraph 0020, lines 4-8; the block 3 in Fig. 1 comprises a current-read resistor, which sends a signal to voltage comparator].

With respect to claim 16, Canova teaches that the current switch includes a MOSFET [[Page 2, paragraph 0020, lines 17-19].

With respect to claim 17, Canova further includes resetting the circuit breaker [Fig. 1, 7] to restore the current flowing in the electrically conductive line [Canova does not disclose a logic-based device as an interrupter (or circuit breaker), but Parker teaches a trip latch 57 as a logic-based device]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Parker into Canova, to reset the trip latch 57 once the cause of the tripping has been determined.

With respect to claim 18, Canova teaches that the step of resetting is performed automatically [Page 1, paragraph 0012, lines 8-10; the microprocessor 13 is programmed to reset the circuit breaker automatically].

With respect to claim 19, Canova further includes generating an indicator signal [Fig. 1, 3] that conveys whether the current is flowing in the electrically conductive line [Page 1, paragraph 0020, lines 4-8; the block 3 in Fig. 1 comprises a current-read resistor, which sends a signal to voltage comparator].

With respect to claim 24, Canova teaches that the current switch includes a MOSFET [Page 2, paragraph 0020, lines 17-19].

3. Claims 5-7, 9, 20, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parker, in view of Huang et al., Patent No. 6,952,335.

Parker teaches an electrically conductive line, but does not disclose that the electrically conductive line is part of an electrical bus energized to at least 60 VDC. Huang teaches a solid-state DC circuit breaker.

With respects to claims 5-7, Huang teaches that the electrically conductive line is part of an electrical bus energized to at least 60, 200 and 300 VDC. [Abstract, liens 1-2, Col. 3, lines 56-57, The DC circuit breaker is capable of interrupting high DC currents, which means the circuit breaker is connected across a high voltage source, which can include 60 VDC, 200 VDC, and 300 VDC].

Both teachings are analogous circuit breakers connected between power supply and loads. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Huang, which teaches high voltage sources, with the circuit of Parker, for the benefit of

providing a circuit breaker that is capable of interrupting high DC currents which come from high DC voltages.

With respect to claim 9, Huang teaches that the sensor includes a Hall effect device [Col. 4, lines 62-67].

With respect to claim 20, Huang teaches that the current flowing in the electrically conductive line is a direct current (DC) [Abstract, lines 1-2].

With respect to claim 22, Huang teaches that the sensor includes a Hall effect current transducer [Col. 4, lines 62-67].

4. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Parker, in view of Yoshida et al., Patent No. 6,791,207.

Parker teaches an electrically conductive line connected to a circuit breaker, and then to the load, but does not disclose that the electrically conductive line is part of a vehicular electrical bus. Yoshida teaches an apparatus for supplying power from a power supply to plural electric loads mounted on an automobile.

With respect to claim 8, Yoshida teaches that the electrically conductive line is a part of a vehicular electrical bus [Col. 2, lines 18-23].

Both teachings are analogous circuit breakers provided between power supply and loads [Col. 2, lines 18-23]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Yoshida, with the circuit of Parker, for the benefit of having double protection or even triple protection against short circuit in an automobile.

Response to Arguments

5. Applicant's arguments filed 10/25/2006 have been fully considered but they are not persuasive.

Applicant comments on page 1 of remarks that there are 1-25 claims pending in the application. There are total of 24 claims in this application.

Applicant comments on page 3 of the remarks that Parker does not disclose or suggest a comparator that compares the voltage level to a reference potential and generates a circuit indicator signal. Parker does teach this limitation. Voltage is one of the components of the signal input to the positive terminal of comparator 55, Figure 2. As shown, Peak Detector 25 takes in line current through Absolute Value 23, and line voltage through Zero Crossing Detector 33 and element 41. Peak Detector 25 then outputs this combined signal to A/D 39, which eventually makes its way to the positive terminal of comparator 55. Therefore the signal inputted to comparator 55 comprises a voltage signal. As shown in Fig. 2, "Line Voltage" is also fed into elements "43" and "47" for processing before being compared with "SDLYTRIPTHRESH" in element "55."

In response to applicant's argument regarding obviousness rejections, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references

would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). The prior art reference Parker does teach the limitation of a comparator comparing the voltage level to a reference potential and generating a circuit indicator signal.

Applicant comments on page 4 of the remarks regarding the rejections of Parker in view of Conova. It is true that Conova does not remedy the deficiency of a comparator, however Parker teaches this limitation as discussed above.

Applicant comments on page 5 of the remarks regarding the rejections of Parker in view of Huang. It is true that Huang does not remedy the deficiency of a comparator, however Parker teaches this limitation as discussed above.

Applicant comments on page 5 of the remarks regarding the rejections of Parker in view of Yoshida. It is true that Yoshida does not remedy the deficiency of a comparator, however Parker teaches this limitation as discussed above.

Based on examiner's best understanding, it is believed that the main prior art reference by Parker reads on the claim language of independent claims 1, 14, and 21.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory

action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dharti H. Patel whose telephone number is 571-272-8659. The examiner can normally be reached on 8:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2800, Ext. 36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service

Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DHP
12/27/2006

Stephen W Jackson
12-28-06

STEPHEN W. JACKSON
PRIMARY EXAMINER